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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,939	10/14/2004	Ting-Shing Wang	11438-US-PA-0P	5938

31561 7590 03/15/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
DANG, PHUC T	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,939	TING-SHING WANG	
	Examiner	Art Unit	
	PHUC T. DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *election filed February 9, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,11,15 and 16* is/are rejected.

7)☒ Claim(s) *3,4,7-10,12-14 and 17-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application is a CIP of 10/605,199 filed on September 15, 2003 which is a CIP of 10/210,031 filed on August 2, 2002 (Patent No. 6,875,653).

Election/Restrictions

2. Applicant's election without traverse of group I (claims 1-22) and canceled group II (claims 23-40) filed on February 9, 2006 has been acknowledged.

Claims 1-22 are currently pending in the application.

Oath/Declaration

3. The oath/declaration filed on October 14, 2004 is acceptable.

Specification

4. On page 6, [paragraph [26]], line 7, " ... the pillar 100 ..." should change to – " ... the pillar 110 ..." --.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was

made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2, 5-6, 11 and 15-16 are rejected under 35 U.S.C. 102 (b) as being anticipated by Schrems (U.S. Patent No. 6,608,341 B2).

Regarding claim 1, Schrems discloses a capacitor for use in a semiconductor memory cell is formed in a substrate comprising:

a semiconductor pillar in Fig. 1 on a substrate 101;

a capacitor on a lower portion 110 of a sidewall of the pillar, comprising:

a first plate 165 in the lower portion 110 of the sidewall of the pillar 160;

a second plate 310 as an upper electrode at periphery of the first plate;

a third plate 161 at periphery of the second plate 310, electrically connecting with the first plate 165 to form a lower electrode together;

a dielectric layer 168 , separating the second plate 310 from the first plate 165 and the third plate 161; and

a vertical transistor in Fig. 5 on an upper portion of the sidewall of the pillar 160, electrically coupled with the capacitor.

Regarding claim 2, Schrems discloses wherein the first plate 165 and the third plate 161 are electrically connected via a design wherein the first plate 165 further extends to the substrate 101 beside the pillar in Fig. 1 and the third plate 161 contacts with the substrate 101 beside the pillar; and the dielectric layer 168 is also disposed on a portion of the first plate 165 in the substrate 101 beside the pillar to separate a bottom of the second plate 310 from the first plate 165.

Regarding claim 5, Schrems discloses the first plate 165, the second plate 310, the third plate 161 and the dielectric layer 164 surround the pillar in Fig. 1.

Regarding claim 6, Schrems discloses the capacitor further comprises: a collar insulating layer 164 surrounding the pillar and covered by an upper portion of the second plate 310 in Fig. 1.

Regarding claim 11, Schrems discloses a capacitor for use in a semiconductor memory cell is formed in a substrate comprising:

rows and columns of memory cells (see col. 1, lines 19-21) disposed on a substrate 101, each comprising:

a semiconductor pillar in Fig. 1 on the substrate 101;

a capacitor on a lower portion of a sidewall of the pillar, comprising a first plate 165 in the lower portion of the sidewall of the pillar, a second plate 310 as an upper electrode at periphery of the first plate 165, a third plate 161 disposed at periphery of the second plate 310 and electrically connected with the first plate 165 to form a lower electrode together, and a dielectric layer 164 separating the second plate 310 from the first plate 165 and the third plate 161; and

a vertical transistor in Fig. 5 on an upper portion of the sidewall of the pillar, electrically coupled with the capacitor;

a plurality of bit lines 185, each coupled with one row of vertical transistors; and

a plurality of word lines 120, each coupled with one column of vertical transistors in Fig. 1.

Regarding claim 15, Schrems discloses in each capacitor, the first plate 165, the second plate 310, the dielectric layer 164 and the third plate 161 surround the pillar in Fig. 3.

Regarding claim 16, Schrems discloses each capacitor further comprises a collar insulating layer 164 that surrounds the corresponding pillar and is covered by an upper portion of the second plate 310 in Fig. 3.

Allowable Subject Matter

6. The following is a statement of reason for the indication of allowable subject matter:

Claim 3-4, 7-10, 12-14 and 17-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the Prior art of record does not disclose the dielectric layer comprises a first dielectric layer between the pillar and the second plate and between the substrate and the second plate; and a second dielectric layer between the second plate and the third plate connecting with the first dielectric layer as cited in claim 3 and the second plate has a top portion directly contacting with a source/drain region of the vertical transistor in the pillar as cited in claim 4 and the second plate comprises a first conductor surrounding the collar insulating layer; a second conductor under the first conductor and the collar insulating layer; and a third conductor on the first conductor and the collar insulating layer, electrically coupled with the vertical transistor as cited in claim 7 and the vertical transistor comprises a first doped region in the sidewall of the pillar electrically connected with the upper electrode of the capacitor;

a second doped region in a top portion of the pillar; a gate on the sidewall of the pillar between the first doped region and the second doped region; and a gate insulating layer between the sidewall of the pillar and the gate as cited in claim 8 and the first plates are electrically connected with each other via a doped surface layer of the substrate between the pillar; the third plates together constitute a conductive layer partially filling the space between the pillars and contacting with the doped surface layer of the substrate and the first plates, the doped surface layer and the conductive layer together serve as a common lower electrode as cited in claim 12 and each second plate has a top portion directly contacting with a source/drain region of a corresponding vertical transistor as cited in claim 14 and the second plate comprises a first conductor surrounding the collar insulating layer; a second conductor under the first conductor and the collar insulating layer; and a third conductor on the first conductor and the collar insulating layer. electrically coupled with a corresponding vertical transistor as cited in claim 17 and each vertical transistor comprises a first doped region in the sidewall of a corresponding pillar, electrically connected with the upper electrode of a corresponding capacitor; a second doped region in a top portion of the pillar; a gate on the sidewall of the pillar between the first doped region and the second doped region; and a gate insulating layer between the sidewall of the pillar and the gate as cited in claim 18.

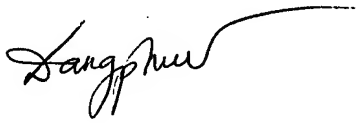
Claims 9-10 are depend on claim 8 and claim 13 is depend on claim 12 and claims 19-22 are directly or indirectly depend on claim 18, then,they also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 571-272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and Final communications.

9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang 

Primary Examiner

Art Unit 2818